CLAIMS

What is claimed is:

1. A method comprising:

in a circuit substrate having a device structure in an active area, filling a portion of a trench with a thermally conducting material;

patterning a thermally conducting contact to the thermally conducting material, wherein the patterned thermally conducting contact has a top surface and a plurality of exposed side surfaces; and

after patterning a thermally conducting contact to the thermally conducting material, forming a spacer portion of dielectric material adjacent to at least one of the exposed side portions.

2. The method of claim 1, further comprising passivating sidewalls of the trench with a dielectric material prior to the step of filling a portion of the trench with a thermally conducting material.

3. The method of claim 1, wherein the thermally conducting material is an electrically insulating material.

4. The method of claim 1, wherein the thermally conducting material is selected from the group consisting of AlN, BN, SiC, polysilicon, and CVD diamond.

5. The method of claim 1, further comprising, after the step of filling a portion of the trench with the thermally conducting material, forming a transistor structure in an active area of the substrate, the transistor structure including a gate on the substrate and diffusion regions in the substrate adjacent the gate.

6. The method of claim 1, wherein the thermally conducting material is a first thermally conducting material, the method further comprising, after forming a spacer portion of dielectric material adjacent to at least one of the exposed side portions, depositing a second thermally conducting material over the structure.

7. The method of claim 6, wherein the first thermally conducting material and the second thermally conducting material are comprised of the same material.

8. A method comprising:

in a circuit substrate having a device structure in an active area, filling a portion of a trench with a first thermally conducting material;

patterning a thermally conducting contact to the first thermally conducting material, wherein the patterned thermally conducting contact has a top surface; and

after patterning a thermally conducting contact to the first thermally conducting material, depositing a second thermally conducting material over the structure.

9. The method of claim 8, further comprising passivating sidewalls of the trench with a dielectric material prior to the step of filling a portion of the trench with a first thermally conducting material.

10. The method of claim 8, wherein the first thermally conducting material and the second thermally conducting material are electrically insulating materials.

11. The method of claim 8, wherein the first thermally conducting material and the second thermally conducting material are selected from the group consisting of AlN, BN, SiC, polysilicon, and CVD diamond.

12. The method of claim 8, wherein the first thermally conducting material and the second thermally conducting material are comprised of the same material.

13. The method of claim 8, further comprising, after the step of filling a portion of the trench with the first thermally conducting material, forming a transistor structure in an active area of the substrate, the transistor structure including a gate on the substrate and diffusion regions in the substrate adjacent the gate.

14. A method comprising:

in a circuit substrate having a transistor structure with a diffusion region in an active area, filling a portion of a trench that is adjacent to the diffusion region with a thermally conducting material;

patterning a first thermally conducting contact to the thermally conducting material; and

patterning a second thermally conducting contact to at least one of the gate and the diffusion region.

15. The method of claim 14, wherein the thermally conducting material has a thermal conductivity greater than 0.183 W/cmK.

16. The method of claim 14, wherein the first thermally conducting contact is electrically insulating.

17. The method of claim 14, wherein the second thermally conducting contact forms an electrical interconnection with at least one of the gate and the diffusion region.

18. The method of claim 17, further comprising a layer of a second thermally conducting material overlying the cell region and adjacent a surface of the second thermally conducting contact.

19. The method of claim 14, wherein the first thermally conducting contact is integrated with the second thermally conducting contact.

20. The method of claim 19, wherein the integrated contact includes a first thermally conducting contact branch to the thermally conducting material and a separate second thermally conducting contact branch to the diffusing region.

21. The method of claim 14, further comprising:

a third contact having a surface, the third contact electrically coupled to the electrical interconnection; and

a third thermally conducting electrically insulating material adjacent the surface of the third contact.

22. A device, comprising:

a semiconductor substrate having a trench surrounding a cell region, wherein a portion of the trench contains thermally conducting electrically insulating material having a thermal conductivity greater than 0.185 W/cmK;

a thermally conducting contact to the thermally conducting electrically insulating material and overlying a portion of the thermally conducting electrically insulating material; and

a circuit device formed in the cell region.

23. The device of claim 22, further comprising a layer of dielectric material on the sidewalls of the trench.

24. The device of claim 22, wherein the thermally conducting electrically insulating material is selected from the group consisting of AIN, BN, SiC, polysilicon, and CVD diamond.

25. The device of claim 22, wherein the thermally conducting contact to the thermally conducting electrically insulating material is a first thermally conducting contact, the device further comprising a transistor structure in the cell region, the transistor structure including a gate on the substrate and diffusion regions in the substrate adjacent the gate, and a second thermally conducting contact to at least one of the gate and the diffusion regions to form an electrical interconnection.

26. The device of claim 25, wherein the first thermally conducting contact is integrated with the second thermally conducting contact.

27. The device of claim 25, wherein the thermally conducting electrically insulating material is a first thermally conducting electrically insulating material and the second thermally conducting contact has a surface, the device further comprising a layer of a second thermally conducting electrically insulating material overlying the cell region adjacent to the surface of the second thermally conducting contact.

28. A device, comprising:

a semiconductor substrate having a trench surrounding a cell region, wherein a portion of the trench contains a first thermally conducting material;

a thermally conducting contact to the first thermally conducting material, wherein the thermally conducting contact has a top surface and a plurality of exposed side surfaces;

a spacer portion of dielectric material adjacent to at least one of the exposed side portions; and

a second thermally conducting material over the structure.

29. The device of claim 28, wherein the first thermally conducting material has a thermal conductivity greater than 0.183 W/cmK.

30. The device of claim 28, wherein the thermally conducting contact is electrically insulating.

31. The device of claim 28, wherein the first thermally conducting material is selected from the group consisting of AIN, BN, SiC, polysilicon, and CVD diamond.

32. The device of claim 28, wherein the thermally conducting contact to the first thermally conducting material is a first thermally conducting contact, the device further comprising a transistor structure in the cell region, the transistor structure including a gate on the substrate and diffusion regions in the substrate adjacent the gate, and a second thermally conducting contact to at least one of the gate and the diffusion regions to form an electrical interconnection.

33. The device of claim 32, wherein the first thermally conducting contact is integrated with the second thermally conducting contact.

34. The device of claim 32, wherein the second thermally conducting contact has a surface, and the second thermally conducting material overlies the cell region adjacent to the surface of the second thermally conducting contact.